

Online Quantization Adaptation for Fault-Tolerant Neural Network Inference

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SafeComp 2023 🕞 BOSCH























Traditional redundancy-based methods
 High overheads (cost, area, power)





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- Adapt to HW faults by retraining NNs

- High overheads (cost, area, power)
- Not possible during runtime





- Traditional redundancy-based methods
- Adapt to HW faults by retraining NNs
- Masking faulty HW elements

- High overheads (cost, area, power)
- Not possible during runtime
- > Not guaranteed to maintain algorithmic performance





Dedicated Hardware Features





Quantization

- Floating-Point \rightarrow Fixed-Point
- Tolerance to reduced precision computations

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Dedicated Hardware Features

Multi-bit-width Support

- E.g., 8-bit and 2x 4-bit
- Increased compute performance and flexibility for different workloads







Dedicated Hardware Features

Lightweight Fault Tolerance

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Method



Method Background – Multi-Bit-Width MAC Unit

Baseline Multiply-Accumulate (MAC) unit:

 $acc = acc + a \cdot b$



Baseline MAC Unit

[1] Beyer, M., Gesper, S., Guntoro, A., Payá-Vayá, G., Blume, H., "Exploiting Subword Permutations to Maximize CNN Compute Performance and Efficiency", 34th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2023.



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With Multi-bit-width support:

 $acc_1 = acc_1 + a_1 \cdot b_1$ $acc_0 = acc_0 + a_0 \cdot b_0$



MAC Unit with Multi-Bit-Width and Subword Permutation Support [1]

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Computations requiring the full precision:

$$a \cdot b = a_1 \cdot b_1 \cdot 2^n + a_1 \cdot b_0 \cdot 2^{\frac{n}{2}} + a_0 \cdot b_1 \cdot 2^{\frac{n}{2}} + a_0 \cdot b_0$$



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Processing Element







Processing Element





Leverage inherent redundancy for lightweight fault tolerance



Processing Element





- Leverage inherent redundancy for lightweight fault tolerance
- Perform computations in fail-degraded operating mode
 → uphold compute capability with reduced precision





Hardware fault

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Method Rounding Modes



Truncate

- Straightforward solution, simple to implement
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Round to Zero

- Preserve overall distribution of weights
- Attenuation rather than overestimation of values





Experiments



Experiments Experimental Setup – Hardware Architecture

Scalable vector processor as HW target



Schematic of the V²PRO Accelerator System [2]

[2] G. B. Thieu et al., "ZuSE-KI-AVF: Application-Specific AI Processor for Intelligent Sensor Signal Processing in Autonomous Driving," in 2023 Design, Automation & Test in Europe Conference & Exhibition (DATE). IEEE, 2023.



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Mapping of convolutions on the V²PRO Accelerator System [2]



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Experiments Experimental Setup – Hardware Architecture

- Scalable vector processor as HW target
- Evaluate different HW configurations



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- ResNet18 [3] & VGG16 [4] (quantized to 8-bit)
 - CIFAR-10 [5] and GTSRB [6]



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- Two error mitigation mechanisms for computations on faulty PEs:
 - 1. OQA: Values are re-quantized online, computations are performed with reduced precision
 - 2. Discard: Values are discarded and set to zero



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Schematic of a box plot. Higher median and lower variability is better.





ResNet18 (CIFAR-10)



Higher median and lower variability is better

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ResNet18 (CIFAR-10)



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ResNet18 (CIFAR-10)



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ResNet18 (CIFAR-10)

VGG16 (CIFAR-10)



Higher median and lower variability is better

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ResNet18 (CIFAR-10)

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ResNet18 (CIFAR-10)

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ResNet18 (CIFAR-10)

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PER in %

PER in %

GTSRB

Higher median and lower variability is better

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6.0

PER in %



VGG16



Higher median and lower variability is better

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VGG16



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Conclusion



 OQA can preserve a NN's classification performance consistently



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- OQA can preserve a NN's classification performance consistently
- Low variability of NN prediction performance
 - Higher confidence in predictions made by NN executed on faulty HW





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- OQA can preserve a NN's classification performance consistently
- Low variability of NN prediction performance
 - Higher confidence in predictions made by NN executed on faulty HW
- NNs retain at least original error-free accuracy when considering top-2 predictions
- Lightweight solution through dual-use of existing HW





Thank you

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References

- [1] M. Beyer, S. Gesper, A. Guntoro, G. Payá-Vayá, H. Blume, "Exploiting Subword Permutations to Maximize CNN Compute Performance and Efficiency", 34th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2023.
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- [3] K. He, et al., "Deep residual learning for image recognition." Proceedings of the IEEE conference on computer vision and pattern recognition. 2016.
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